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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :
H04B 1/38, H03H 7/30, H04M 1/24, H04J 1/00

A1

(11) International Publication Number: WO 95/17046

(43) International Publication Date: 22 June 1995 (22.06.95)

(21) International Application Number: PCT/US94/14250

(22) International Filing Date: 12 December 1994 (12.12.94)

(30) Priority Data:
08/169,810 17 December 1993 (17.12.93) US

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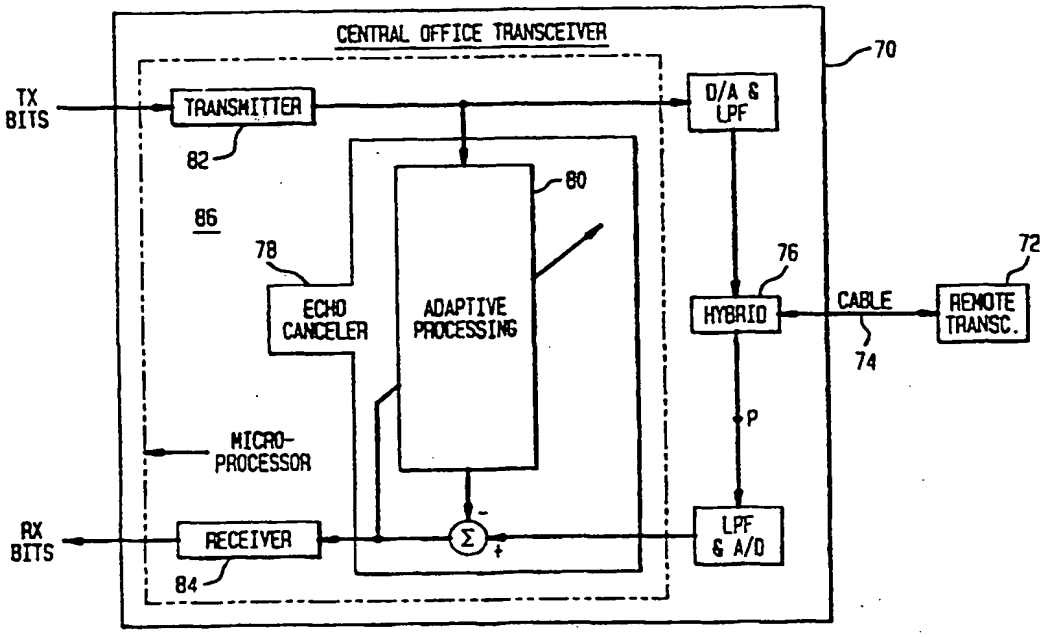
(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: AN IMPROVED DISCRETE MULTITONE ECHO CANCELER



(57) Abstract

Echo cancellation can be used to increase the reach or noise margin of a channel to make use of the low frequency portion of the cable spectrum. A generalization of previously described cancelers, when properly optimized, results in significant complexity reduction. The generalization applies to the Cyclic Echo Synthesizer (CES), which forms the time-domain processing portion of the canceler. By expanding the achievable CES input range and optimizing the temporal alignment between transmitter (82) and echo canceler (78), canceler computational complexity is reduced.

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AN IMPROVED DISCRETE MULTITONE ECHO CANCELER

Background and Summary of the Invention

An Asymmetric Digital Subscriber Line (ADSL) is an emerging technology for the transport of Video Dial Tone (VDT) and other new services over the copper local loop plant. See, for example: D. Waring, "The Asymmetrical Digital Subscriber Line (ADSL): A New Transport Technology for Delivering Wideband Capabilities to the Residence," Proc. Globecom '91, Phoenix, AZ, pp. 1979-1986, Dec. 5, 1991; Also see: T. R. Hsing, C. T. Chen, and J. A. Bellisio, "Video Communications and Services in the Copper Loop," IEEE Communications Magazine, vol. 31, no. 1, pp. 62-68, January 1993).

ADSL will provide between one and four unidirectional DS1-rate (1.544 Mbps) channels in the downstream direction (from central office to customer) and one or more lower-speed bidirectional channels in both upstream and downstream directions, all in addition to analog Plain Old Telephone Service (POTS). This asymmetry is designed into ADSL because it extends the achievable service range while still providing the transport required for many high bit-rate services. For example, in VDT systems, the unidirectional DS1s would carry "VCR quality" compressed video channels to the customer, while the customer's control of and response to the video channels would be adequately carried by one of the bidirectional control channels. The service range extension produced by the asymmetry occurs because of the greatly reduced level of self Near End Crosstalk (self Next) with which the remote receiver must contend.

Discrete Multitone (DMT) modulation has been selected by the American National Standards Institute (ANSI) T1E1.4 committee as the modulation format for ADSL (see: B. R. Saltzberg, "Performance of an Efficient Parallel Data Transmission System," IEEE Transactions on Communication Technology, vol. COM-15, no. 6, December 1967, pp. 805-81; see also: A. Peled and A. Ruiz, "Frequency Domain Data Transmission using Reduced Computational Complexity Algorithms," Proceedings of the International Conference on Acoustics, Speech, and Signal Processing, April 1980, Denver, pp. 964-967; see also: J. A. C. Bingham, "Multicarrier Modulation for Data Transmission: An Idea Whose Time Has Come," IEEE Communications Magazine, vol. 28, no. 4, May 1990, pp. 5-14).

DMT efficiently implements multi-QAM modulation, i.e., the transmit signal is a sum of N/2 independent QAM waveforms. Quadrature Amplitude Modulation, or QAM, is a modulation technique well known in the art in which information is conveyed through the magnitude and phase of a transmitted cosine waveform at a specified carrier frequency. Multi-QAM transmits information through a sum of such QAM waveforms, whose carrier frequencies are such that the constituent cosine waveforms can be separated from one another and processed by the receiver. The carrier frequencies of the multiple QAM channels are evenly spaced by an Inverse Fast Fourier Transform (IFFT) modulator. Each symbol period, the transmit coder gathers a block of B bits and maps these into the set of complex magnitude/phase indicators. The DMT transmit signal during the symbol period is a continuous-time waveform of a specific duration, which is specified precisely by its samples taken at a particular sampling rate.

For a DMT receiver, the received signal is sampled at the same sampling rate that was used in the transmitter. A Time

Domain Equalizer (TEQ) may be present in the DMT receiver. A TEQ is a Finite Impulse Response (FIR) filter used to shorten the length of the overall channel impulse response. The TEQ works with a Cyclic Prefix to mitigate intersymbol interference. The receive Cyclic Prefix samples correspond to the transmitted Cyclic Prefix samples, and are discarded. The remaining samples for the symbol are applied to an FFT.

Given the FFT output vector, a Frequency Domain Equalizer (FEQ) and Slicer block form an estimate of the ith transmitted QAM cosine waveform magnitude / phase variable. It does this by compensating for the distortion applied to each QAM signal by the channel, and hard-limiting to the QAM constellation grid. The decoder then regenerates the bits originally encoded at the transmitter.

In DMT-based ADSL, or any other full duplex copper loop transmission system, echo cancellation can be used to improve the transport performance. Here, a "full-duplex" transmission system refers to one in which the two transceivers at opposite ends of the link transmit simultaneously, even though only one wire pair transmission line connects the two ends. Thus, in a full duplex system the signal present on the transmission line is a combination of the two transmit signals from the opposite ends. For example, the signal present on the wire pair can be a superposition of the Central Office and Remote Transceivers' transmit signals.

For proper operation, each receiver requires that only the transmit signal from the opposite end be present at its input. The suppression of the Central Office Transceiver transmit signal at the Central Office Receiver input is accomplished by a hybrid / echo canceler combination. Similarly, the suppression of the Remote transceiver's transmit signal at the Remote receiver input is performed by

its own hybrid / echo canceler pair. A hybrid is a balance network, known in the art, which, when perfectly matched to the transmission line impedance, couples all of the local transceiver's transmit signal onto the line. When the hybrid balance impedance does not perfectly match that of the transmission line, the signal at each receiver's input will remain a combination of the transmit signals from both Central Office and Remote Transceivers.

For systems like ADSL in which the transmission line characteristics are unknown a priori, some hybrid mismatch can be expected most of the time. For such cases an echo canceler can be used to remove that portion of the local transmit signal which remains at the receiver input. This is accomplished through knowledge of the local transmit signal and the echo impulse response, the latter being learned by the echo canceler through adaptive signal processing techniques. Using knowledge of the local transmit signal and echo impulse response, adaptive processing generates a replica of the local transmitter portion of the signal. This replica is then subtracted from the hybrid output signal, leaving only the far-end transmit signal present at the local receiver input.

While Digital Subscriber Line (DSL) and High-Speed Digital Subscriber Line (HDSL) transceivers achieved enhanced performance through the use of echo cancellation, the first ADSL prototypes separated the upstream and downstream signals spectrally using frequency domain multiplexing (FDM). The rationale for this departure was based on the asymmetric aspect of ADSL. With original ADSL prototype target rates of approximately 1.6 Mbps downstream and 16 kbps upstream, the loss of available downstream bandwidth in an FDM system seemed worth the complexity reduction achieved through elimination of an echo canceler. DSL, HDSL, and FDM are known in the art. See, for example, American National Standards Institute ANSI

T1.601, Integrated Services Digital Network (ISDN) - Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification); R.C. McConnell, "High-Bit-Rate Digital Subscriber Lines (HDSL)," ANSI T1E1.4/92-002R2, June 30, 1992; B. A. Blake, "Results of Transmission Tests on an ADSL Transceiver Prototype," ANSI T1E1.4/93-030, March 3, 1993.

The emergence of a higher speed ADSL, sometimes called ADSL3, with a Carrier Serving Area (CSA) range, has since generated interest in echo cancellation for ADSL. CSA loops have a total length, including the length of any attached bridge taps, limited to 12 kft for 24 AWG gauge wire, or 9kft for 26 AWG gauge wire. For with maximum ADSL3 downstream and upstream rates approaching 7 Mbps and 450 kbps, respectively, CSA coverage may require the use of an echo canceled system. See, for example, J. M. Cioffi, J. T. Aslanis, and M. Ho, "Performance of Enhanced (6 Mbps) ADSL," ANSI T1E1.4/92-205, December 1, 1992. (See, for example, J. A. C. Bingham and J. M. Cioffi, "Recommended CSA Range 6 Mbps Service for DMT ADSL," ANSI T1E1.4/93-112, May 10, 1993.) As a result, suitable processing schemes for DMT-based ADSL echo cancellation are of considerable interest. In particular, echo canceler structures which are computationally efficient, yet achieve high cancellation performance, deserve careful study.

Such a canceler is known in the prior art. Because this canceler involves signal processing in both the time and frequency domains, it will be referred to henceforth as the Time and Frequency Domain Echo Canceler (TAFDEC). See, for example, J. M. Cioffi and J. A. C. Bingham, "Echo Cancellation for ADSL," ANSI T1E1.4/93-020, March 8, 1993; also see: J. M. Cioffi and J. A. C. Bingham, "A Data-Driven Multitone Echo Canceler," Proceedings of the IEEE Global Telecommunications Conference, Phoenix, Arizona, 1991; also see: M. Ho, J. M.

Cioffi, and J. A. C. Bingham, "An Echo Cancellation Method for DMT with DSLs," ANSI T1E1.4/92-201, December 1, 1992.

The prior art TAFDEC uses a Cyclic Echo Synthesizer (CES) as its time domain processing element. The function of the CES is to produce an output echo signal which appears to have arisen from a periodic transmit signal. Such an echo signal can then be canceled efficiently in the frequency domain. However, a practical implementation of a CES may be very complex (i.e. require a relatively large number of computations), and hence require a relatively large amount of computing resources. It is desirable to reduce the complexity of the CES.

According to the present invention, a Digital Multitone transceiver, for transmitting and receiving digital messages on the same channel, has a hybrid, coupled to the channel, a transmitter, including a parallel to serial converter, the transmitter being coupled to the hybrid to provide message signals to the hybrid, an echo canceler, coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a received message signal, the echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, the echo canceler subtracting, in the frequency domain, a signal indicative of a signal provided by the transmitter, and a receiver, including a serial to parallel converter, the receiver being coupled to the echo canceler to provide an output signal, wherein the serial to parallel and parallel to serial converters are set to provide a non-zero phase difference between signals of the transmitter and receiver and wherein the phase shift and multiply provided by the echo canceler compensate for the phase difference. The Digital Multitone transceiver can be configured such that the

phase difference is set to a value that minimizes the complexity of the echo canceler.

According further to the present invention, Digital Multitone transceiver, for transmitting and receiving digital messages on the same channel, has a hybrid, coupled to the channel, a transmitter, including a parallel to serial converter, the transmitter being coupled to the hybrid to provide message signals to the hybrid, an echo canceler, including a serial to parallel converter, the echo canceler being coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a received message signal, the echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, the echo canceler subtracting, in the time domain, a signal indicative of a signal provided by the transmitter; and a receiver, the receiver being coupled to the echo canceler to provide an output signal, the serial to parallel and parallel to serial converters being configured to provide a non-zero phase difference between signals of the transmitter and the echo canceler and wherein the phase shift and multiply provided by the echo canceler compensate for the phase difference. The Digital Multitone transceiver can be configured such that the phase difference is set to a value that minimizes the complexity of the echo canceler.

The prior art TAFDEC requires that there be perfect temporal alignment between the transmit and receive symbol boundaries at the Remote Transceiver. The features of the invention make it possible to establish any desired temporal misalignment. In addition, the features of the invention allow proper operation with any selected misalignment. Furthermore, there exists an optimal misalignment value which minimizes complexity of the CES and is considerably different from the value of zero required in the prior art TAFDEC. The

new TAFDEC described herein can use any misalignment value, including the optimal one, and thereby achieve performance superior to that available from the prior art. As a result, when based on identical implementation processors, the improved TAFDEC described in this report achieves higher performance than that of the prior art by canceling a greater percentage of the total echo energy. The ability of the improved TAFDEC to work with any canceler/transmitter misalignment approximately doubles the achievable performance, relative to that of the prior art (i.e., zero misalignment).

Brief Description of Drawings

FIG. 1 is a schematic block diagram of a Discrete Multitone transmitter.

FIG. 2 is a schematic block diagram of a Discrete Multitone Receiver.

FIG. 3 is a schematic block diagram of a Transceiver with echo cancellation.

FIG. 4 is a graphic representation illustrating temporal misalignment of Discrete Multitone symbols.

FIG. 5 is a schematic block diagram of a remote ASDL DMT transceiver (ATU-R) having a relatively high receive rate and a relatively low transmit rate.

FIG. 6 is a plot of CES multiplications (complexity) vs. Symbol misalignment for a Shared-FFT TAFAEC ATU-R of FIG. 5.

FIG. 7 is a schematic block diagram of a Central Office ASDL DMT transceiver (ATU-C) having a relatively low receive rate and a relatively high transmit rate.

FIG. 8 is a plot of CES multiplications (complexity) vs. Symbol misalignment for a Shared-FFT TAFDEC ATU-C of FIG. 7.

FIG. 9 is a schematic block diagram of a Central Office ASDL DMT transceiver (ATU-C) having a separate FFT echo canceler.

FIG. 10 is a plot of CES multiplications (complexity) vs. Symbol misalignment for a separate FFT TAFDEC ATU-C of FIG. 9.

FIG. 11 is a schematic block diagram of a Symmetric DMT transceiver having a shared FFT echo canceler.

FIG. 12 is a schematic block diagram of a Symmetric DMT transceiver having a separate FFT echo canceler.

Detailed Description of Drawings

Referring to FIG. 1, a schematic block diagram shows a DMT transmitter 30 for providing an analog TRANSMIT SIGNAL that varies according to the digital TRANSMIT BITS that are provided to the transmitter 30. Implementation of the transmitter 30 will be discussed in more detail hereinafter.

The TRANSMIT BITS signal is provided to a coder 32, which maps the bits of the signal into a plurality of QAM waveforms (QAM channels), each having a different carrier frequency. The carrier frequencies of the QAM waveforms are such that the constituent cosine waveforms can be separated from one another and processed by the receiver. The carrier frequencies of the multiple QAM channels are evenly spaced by an Inverse Fast Fourier Transform (IFFT) modulator 34. Each symbol period, the transmit coder gathers a block of B bits and maps these into the set of complex magnitude/phase indicators $\{U_0^n, U_1^n, \ldots, U_{N/2}^n\}$.

That is, during symbol period number n, the magnitude and phase of the ith component QAM signal at the transmitter output is equal to the magnitude and phase of the complex number U_i^n. The remaining coder outputs, $\{U_{(N+2)/2}^n, \ldots, U_{N-1}^n\}$, by design of the coder will satisfy:

$$U_i^n = (U_{N-i}^n)^*, \quad i=(N+2)/2,(N+4)/2,\ldots,N-1 \qquad (1)$$

which forces the output samples of the IFFT 34 to be strictly real.

The DMT transmit signal during symbol period n is a continuous-time waveform of duration $T=(N+\nu)\tau$, which is specified precisely by its samples taken at the sampling rate $f_s = 1/\tau$. These samples are the elements of the sequence $\{\tilde{u}^n_{N-\nu}, \tilde{u}^n_{N-\nu+1}, \ldots, \tilde{u}^n_{N-1}, \tilde{u}^n_0, \ldots \tilde{u}^n_{N-1}\}$ shown in Fig. 1. A cyclic prefix generator 36 provides the first ν samples of a transmit symbol (the Cyclic Prefix (CP) samples) which are identical to the last ν samples of the symbol. The transmission of a Cyclic Prefix is a common means for overcoming intersymbol interference in DMT systems. See, for example, J. S. Chow, "Finite-Length Equalization for Multi-Carrier Transmission Systems," Ph. D. dissertation, Stanford University, June 1992.

The last N samples of the transmit symbol are the IFFT of the coder output vector $\{U^n_0, U^n_1, \ldots, U^n_{N-1}\}$, and are given by:

$$\tilde{u}^n_k = \frac{1}{N}\sum_{i=0}^{N-1} U^n_i e^{+j2\pi ki/N}, \quad k=0,1,\ldots,N-1 \qquad (2)$$

A Parallel-to-Serial converter (P/S) 38 causes the sequence of samples $\{\tilde{u}^n_{N-\nu}, \tilde{u}^n_{N-\nu+1}, \ldots, \tilde{u}^n_{N-1}, \tilde{u}^n_0, \ldots \tilde{u}^n_{N-1}\}$ to appear, in the specified order, at the input to a D/A converter 40. Following the second application of $\tilde{u}^n_{N-1}$ to the converter 40, the next symbol period begins, and the above process is repeated.

Referring to FIG. 2, a schematic block diagram shows a DMT receiver 50 which is provided an analog RX SIGNAL and provides a digital RX BITS signal. Implementation of the DMT receiver is discussed in more detail hereinafter.

The received signal is first provided to a Low-Pass filter & A/D converter combination 52. The signal is sampled at the same sampling rate $f_s = 1/\tau$ that was used in the transmitter. A Time Domain Equalizer (TEQ) 54 may be present

in the DMT receiver 50. A TEQ is a Finite Impulse Response (FIR) filter used to shorten the length of the overall channel impulse response to approximately ν samples. The output of the TEQ 54 is provided to a Serial-to-Parallel converter 56.

The TEQ 54 works with the Cyclic Prefix to mitigate intersymbol interference. The receive samples $\gamma_{-\nu}^{n}, \ldots \gamma_{-1}^{n}$ that are output by the Serial-to-Parallel converter 56 correspond to the transmitted Cyclic Prefix samples, and are discarded. The remaining samples for symbol n, namely, $\{\gamma_0^n, \gamma_1^1, \ldots, \gamma_{N-1}^n\}$, are applied to an FFT 58, the output of which is:

$$\Gamma_i^n = \sum_{k=0}^{N-1} \gamma_k^n e^{-j2\pi ki/N}, \quad i = 0,1,\ldots,N-1 \qquad (3)$$

The output vector of the FFT 58 is applied to a Frequency Domain Equalizer (FEQ) and Slicer block 60 which forms an estimate of the ith transmitted QAM cosine waveform magnitude/phase variable $\hat{U}_i^n$. The FEQ and Slicer block 60 does this by compensating for the distortion applied to each QAM signal by the channel, and hard-limiting to the QAM constellation grid. A decoder 62 then regenerates the B bits originally encoded at the transmitter 30.

In DMT-based ADSL, or any other full duplex copper loop transmission system, echo cancellation can be used to improve the transport performance. Here, a "full-duplex" transmission system refers to one in which the two transceivers at opposite ends of the link transmit simultaneously, even though only one wire pair transmission line connects the two ends. Thus, in a full duplex system the signal present on the transmission line is a combination of the two transmit signals from the opposite ends.

Referring to Fig. 3, a central office transceiver 70 is connected to a remote transceiver 72 via a cable 74. The cable 74 can be a wire pair, a fiber-optic cable, or a variety of other similar communication means known to one of ordinary skill in the art. The signal present on the cable 74 is a superposition of transmit signals of both the central office transceiver 70 and the remote transceiver 72.

For proper operation, the receiver portion of each transceiver 70,72 requires that only the transmit signal from the other one of the transceivers 70,72 be present at the receiver input. The signal from the cable 74 is provided to a hybrid 76 which is part of the transceiver 70. A hybrid is a balance network, known in the art, which, when perfectly matched to the transmission line impedance, couples all of the local transceiver's transmit signal onto the line. The hybrid 76 separates the signal transmitted by the transceiver 70 from the signal on the cable 74 in order to provide a received signal at a point P shown in FIG. 3.

When the hybrid balance impedance does not perfectly match that of the transmission line, the signal at point P will remain a combination of the transmit signals from both the central office transceiver 70 and remote transceiver 72. For systems like ADSL in which the transmission line characteristics are unknown a priori, some hybrid mismatch can be expected most of the time. For such cases an echo canceler 78 can be used to remove that portion of the local transmit signal which remains at point P. This is accomplished through knowledge of the local transmit signal and the echo impulse response, the latter being learned by the echo canceler 78 through adaptive signal processing techniques. Using knowledge of the local transmit signal and echo impulse response, an Adaptive Processing block 80 generates a replica of the local transmitter portion of the signal at point P. The replica is

then subtracted from the output signal of the hybrid 76, leaving only the far-end transmit signal present at the local receiver input.

Suppression of the transmit signal of the central office transceiver 70 at the central office Receiver input is accomplished by the hybrid 76 and echo canceler 78 combination, as shown. Similarly, the suppression of the Remote transceiver's transmit signal at the Remote receiver input is performed by its own hybrid / echo canceler pair.

The transceiver 70 also includes a transmitter 82 and a receiver 84 similar to the DMT transmitter 30 shown in FIG. 1 and the DMT receiver 50 shown in FIG. 2, respectively. The transmitter 82, receiver 84, and echo canceler 78 can be implemented by one of ordinary skill in the art using a microprocessor system 86 and software, including associated ROM (not shown), RAM (not shown), interface circuitry (not shown), etc. Therefore, the detailed discussion which follows will focus on a microprocessor software implementation. However, it will be understood by one of ordinary skill in the art that it is possible to provide equivalent functionality using hardware for some or all of the software that is described herein.

The echo canceler 78 involves signal processing in both the time and frequency domains, and hence is referred to as a Time and Frequency Domain Echo Canceler (TAFDEC). Such cancelers are described in the prior art. See, for example, J. M. Cioffi and J. A. C. Bingham, "Echo Cancellation for ADSL," ANSI T1E1.4/93-020, March 8, 1993; also see: J. M. Cioffi and J. A. C. Bingham, "A Data-Driven Multitone Echo Canceler," Proceedings of the IEEE Global Telecommunications Conference, Phoenix, Arizona, 1991; and M. Ho, J. M. Cioffi, and J. A. C. Bingham, "An Echo Cancellation Method for DMT

with DSLs," ANSI T1E1.4/92-201, December 1, 1992, which are both incorporated by reference herein.

The prior art TAFDEC uses a Cyclic Echo Synthesizer (CES) as its time domain processing element. The function of the CES is to produce an output echo signal which appears to have arisen from a periodic transmit signal. Such an echo signal can then be canceled efficiently in the frequency domain.

Referring to Fig. 4, a time line 90 shows two possible temporal misalignment values, Ψ, between an ADSL transceiver's transmit and receive symbol boundaries. The CP and IFFT portions of a transmit symbol refer to the CP and IFFT samples, respectively, which make up that symbol. Similarly for the received symbol, the CP and FFT portions refer to the discarded CP samples and the FFT input samples, respectively. In Fig. 4, "misalignment" means the offset between the beginning of the "present" transmit and receive symbols. For a positive misalignment $(\Psi>0)$, the echo contained within the present received symbol may, depending on the echo impulse response, contain contributions from the previous, present, and next transmit symbols. For $\Psi<0$, the echo is due to the previous and present transmit symbols only. The goal of the CES in either case is to make the received echo appear as though the "present" transmit symbol were always sent, in which case the transmit signal would be periodic. As shown elsewhere herein, the CES does this through knowledge of the transmit samples and the echo impulse response.

The prior art TAFDEC CES processes samples from only the present and previous transmit symbols, and will thus be referred to as a "backward-only" CES. As discussed in P. J. W. Melsa and R. C. Younce, "Performance of Echo Cancellation for ADSL," ANSI T1E1.4/93-203, August 23, 1993, generalization of the TAFDEC can be accomplished by expanding

the input range of the CES, so that the next transmit symbol can be processed as well. This generalized CES will be called a "forward-backward" CES. A reasonable amount of pipelining at the transmitter allows for such an implementation. For example, assume that the transmitter computations are such that the samples of the "next" transmit symbol are computed and stored while the samples from the "present" transmit symbol are being transmitted onto the line. Thus by the time the first sample of the "next" transmit symbol is due to be transmitted, all of the samples of that "next" transmit symbol are assumed available. As a result, a forward-backward CES does not require any noncausal processing, but is instead an implementable device. As illustrated in Fig. 4, it is possible for a given transceiver's symbol boundaries to either be in perfect temporal alignment, or be are misaligned by some amount.

Referring to Fig. 5, a remote ASDL transceiver (ATU-R) 100 uses an improved TAFDEC. The transceiver 100 can represent any asymmetric DMT transceiver which contains a high speed receiver and a low speed transmitter. The improvement in this TAFDEC relative to the prior art is in its ability to establish and work properly with any specified transmit/receive symbol misalignment value.

Due to the transmission asymmetry in ADSL, the ATU-R 100 utilizes a multi-rate DSP implementation. The ATU-R 100 contains a low-speed transmitter 102, with sampling rate of 276 kHz, and a high speed receiver 104, with sampling rate 2208 kHz (8 times faster than the low-speed rate). However, it will be appreciated by one of ordinary skill in the art that the discussion which follows can be applicable to any asymmetric DMT transceiver having a relatively high speed receiver and a relatively low speed transmitter.

A downstream demodulator 106 uses an FFT 108 of size five hundred and twelve samples, plus a thirty-two sample cyclic prefix. The corresponding upstream numbers, measured in low speed samples, are one-eighth those of the downstream case. As a result, measured in real time, the upstream and downstream symbol periods are equal.

In Fig. 5, the superscript n_T or n_R on a quantity bearing such refers to the value of the quantity during the symbol period indicated by the superscript. For quantities which bear a superscript, the corresponding subscript refers to the sample number within that symbol period. Quantities with subscripts only are time-indexed through the subscript alone. For example, $\tilde{u}^{n_T}_{k_T} = f_{68}n_T+k_T$ is the $k_T th$ low-speed upstream transmit sample of the ATU-R 100 during transmit symbol period n_T. The low-speed upstream transmit samples are generated, as shown, by a sixty-four-point IFFT 110. The samples $\tilde{u}^{n_T}_{k_T}$, and other quantities with a tilde in later figures, are, for a fixed value of their superscript, periodic functions of their subscripts. The period in each case is equal to the length of the IFFT which generates the periodic quantity. This notation is a concise means of showing the upstream Cyclic Prefix output to be the last four outputs of the IFFT.

In Fig. 5 the ability of the transceiver 100 to use any misalignment value Ψ is indicated by the presence of separate transmitter and receiver superscript/subscript pairs, (n_T,k_T) and (n_R,k_R), respectively. To achieve a desired misalignment value Ψ, the designer sets the relative phase between P/S_U and S/P_G such that:

$$(n_T, k_T) = \begin{cases} \left(n_R - 1, \left\lfloor \frac{k_R + \Psi + 544}{8} \right\rfloor\right), & k_R \le -33 - \Psi \\ \left(n_R, \left\lfloor \frac{k_R + \Psi}{8} \right\rfloor\right), & -32 - \Psi \le k_R \le 511 - \Psi \\ \left(n_R + 1, \left\lfloor \frac{k_R + \Psi - 544}{8} \right\rfloor\right), & k_R \ge 512 - \Psi \end{cases} \quad (4)$$

where by definition:

$$\lfloor x \rfloor = \text{greatest integer} \le x \quad (5)$$

This is accomplished as follows: The phase of S/P_G is first set so as to align with that of the received symbol boundary sent from the ATU-C (the far-end transceiver). The phase of P/S_U is then set at a certain offset from that of S/P_G so as to implement (4) for the desired Ψ. For example, say that a value of $\Psi = 10$ is desired. Then P/S_U should be phased so that $\tilde{u}^n_{-4}$, is newly applied to the D/A input at the same time that g_{502}^{n-1} is at the input to S/P_G. Then $\tilde{u}^n_{-3}$ is newly applied to the D/A input at the same time that g_{510}^{n-1} is at the input to S/P_G, and so on.

In Fig. 5, the TAFDEC processing is performed by a CES 112 and a Frequency Domain Echo Canceler (FDEC) 114. The other portions of the transceiver 100 are similar to portion S shown in connection with in Fig. 1 or 2 and have been previously described. The TAFDEC processing of Fig. 5 also makes use of the FFT 108, the use of which it shares with the receiver demodulator 106. As a result, the TAFDEC structure of Fig. 5 is referred to as a "shared-FFT" TAFDEC.

The operation of the "shared-FFT" canceler of Fig. 5 is now described. It is assumed that the D/A and A/D sample clocks, while differing in frequency by a factor of eight, are

clocks, while differing in frequency by a factor of eight, are phase-locked. Assume that a nominal misalignment of Ψ, samples is established between P/S_U and S/P_G. As described in D. C. Jones, "Consequences of Asynchronous Sample Clocking for a DMT ADSL Frequency Domain Echo Canceler," ANSI T1E1.4/93-168, August 24, 1993, the use of an asynchronous sample clocking timing recovery scheme will produce a small amount of jitter in the misalignment value, which the receiver 104 can track exactly. In a loop-timing synchronization scheme, no such jitter is introduced. In loop-timing, the Remote Transceiver A/D and D/A sampling clocks are phase-locked to one another, and, through the use of a Phase-Locked Loop (PLL), also phase-locked to the Central Office Transceiver sampling clock.

Since the invention described herein applies equally well to all timing recovery schemes, the misalignment will be described in most general terms as Ψ_n, where Ψ_n is the misalignment in effect during symbol number n. Assume that the high-speed samples of the echo impulse response are given by h_{echo_k}, and that h_{echo_k} is known to be zero for all k outside the interval $[E_L, E_U]$. For a high-speed DMT FFT length of N=512, assume that $E_L \geq 0$ and $E_U \leq 511$. Subject to these assumptions, then with the ATU-C silenced and no channel noise it can be shown that:

$$g_k^n = \sum_{m=E_L'(k)}^{\min(-64,E_U'(k))} h_{echo_{8m+\Psi_n+k}} \bar{u}_{-68-m}^{n+1} + \sum_{m=\max(-63,E_L'(k))}^{\min(4,E_U'(k))} h_{echo_{8m+\Psi_n+k}} \bar{u}_{-m}^{n} + \sum_{m=\max(5,E_L'(k))}^{E_U'(k)} h_{echo_{8m+\Psi_n+k}} \bar{u}_{68-m}^{n-1}, \quad 0 \leq k \leq 511 \qquad (6)$$

where by definition

EQ (7)

$$E_L'(k) = \left\lfloor \frac{E_L + 7 - \Psi_n - k}{8} \right\rfloor \qquad (7)$$

$$E'_U(k) = \left\lfloor \frac{E_U - \Psi_n - k}{8} \right\rfloor \quad (8)$$

The function to be performed by the CES 112 in this improved TAFDEC processing is to form the output:

$$q_k^n = g_k^n - \varepsilon_k^n, \; 0 \le k \le 511 \quad (9)$$

where by definition:

$$\varepsilon_k^n = \sum_{m=E'_L(k)}^{\min(-64, E'_U(k))} h_{echo_{8m+\Psi_n+k}} (\tilde{u}_{-68-m}^{n+1} - \tilde{u}_{-64-m}^{n})$$

$$+ \sum_{m=\max(5, E'_L(k))}^{E'_U(k)} h_{echo_{8m+\Psi_n+k}} (\tilde{u}_{68-m}^{n-1} - \tilde{u}_{64-m}^{n}), \; 0 \le k \le 511 \quad (10)$$

The echo contained in the output of the CES 112 will then be given by:

$$\text{Cyclic Echo} = \sum_{m=E'_L(k)}^{E'_U(k)} h_{echo_{8m+\Psi_n+k}} \tilde{u}_{-m}^{n}, \; 0 \le k \le 511$$

$$= \sum_{m=E_L}^{E_U} h_{echo_m} \tilde{\sigma}_{k+\Psi_n-m}^{n}, \; 0 \le k \le 511 \quad (11)$$

This echo component in the output of the CES 112 is canceled by the FDEC 114, which forms the output:

$$W_K^n = Q_k^n - e^{+j2\pi k \Psi_n / 512} H_{echo_k} U_{k \bmod 64}^n, \; 0 \le k \le 256 \quad (12)$$

The TAFDEC processing of Fig. 5 can obtain an initial estimate of H_{echo_k} by applying a periodic training sequence $\tilde{u}_k$ with no cyclic prefix, and forming:

$$\hat{H}^{0}_{echo_m} = \text{Average}(Q_m)/U_{m \bmod 64},\ 0 \le m \le 511 \qquad (13)$$

An initial echo estimate can also be set to zero. Following initialization, periodic updates of the echo estimate are via the LMS algorithm:

$$\hat{H}^{n+1}_{echo_m} = \hat{H}^{n}_{echo_m} + \mu e^{-j2\pi\Psi_n m/512} U^{n*}_{m \bmod 64} W^{n}_{m},\ 0 \le m \le 511 \qquad (14)$$

It is possible to reduce the computational complexity of a forward-backward CES for the shared-FFT echo canceler. Note that, although this example uses the forward-backward CES 112 of FIG. 5, the technique described hereinafter is also applicable to the use of a backward-only CES, as the backward-only case is just a special case of the more general forward-backward analysis.

The discussion below will demonstrate how the computational complexity required for the CES 112 is a function of the symbol misalignment value in use. Also, it will be shown that a certain nonzero misalignment value yields a minimum CES complexity, which is approximately half that of the prior art (i.e., zero misalignment).

The following results can be proven. (See, for example, D. C. Jones, "Reducing the Complexity of a Cyclic Echo Synthesizer for a DMT ADSL Frequency Domain Echo Canceler," ANSI T1E1.4/93-255, October 4, 1993.) Assume that the samples of a given received symbol are offset from the present transmit symbol by an amount Ψ_n. Assume that echo contributions to the present received symbol samples come only from the present, previous, and next transmit symbols. Denote N_{prev} as the number of CES multiplications required, for the

present received symbol, to process echo due to the previous transmit symbol. Denote N_{next} as the number of CES multiplications required, for the present received symbol, to process echo due to the next transmit symbol. Consideration of three distinct cases of Ψ_n *for* N_{prev} .

Case 1: $E_L-551 \le \Psi_n \le E_L-41$

In this case,

$$N_{prev} = 4\cdot\left\lfloor \frac{E_U-E_L}{8} \right\rfloor \cdot \left\lfloor \frac{E_U-E_L+8}{8} \right\rfloor + \left\lfloor \frac{E_U-E_L+8}{8} \right\rfloor \cdot [1+(E_U-E_L) \bmod 8]$$
$$+ \frac{1}{8} \sum_{k=0}^{(E_L+7-\Psi_n) \bmod 8} [k - (E_U-\Psi_n-k) \bmod 8] + \frac{(E_U-E_L+1)(E_L-\Psi_n-40)}{8} \quad (15)$$

Case 2: $E_L-40 \le \Psi_n \le E_U-40$

For this case,

$$N_{prev} = 4\cdot\left\lfloor \frac{E_U-\Psi_n-40}{8} \right\rfloor \cdot \left\lfloor \frac{E_U-\Psi_n-32}{8} \right\rfloor$$
$$+ \left\lfloor \frac{E_U-\Psi_n-32}{8} \right\rfloor \cdot [1+(E_U-\Psi_n) \bmod 8] \quad (16)$$

Case 3: $E_U-39 \le \Psi_n \le 512$

In this case,

$$N_{prev} = 0 \quad (17)$$

It can also be shown that:

$$N_{next}(\Psi) = N_{prev}(E_U+E_L-39-\Psi) \quad (18)$$

where the dependence of N_{prev} and N_{next} on Ψ has been made explicit. Using (15)-(18), Figure 6 shows how $N_{total}=N_{prev}+N_{next}$ varies with Ψ_n *for* E_L = *0* and E_u = one hundred, two hundred, two hundred and fifty, and three hundred.

The accuracy of (15)-(18) has been verified for these values of (E_L, E_u) using a simulation routine.

Referring to Fig. 6, the optimal value of Ψ_n is slightly less than Ψ_n, at which point the required CES complexity is roughly half that of the prior art (i.e., the zero misalignment case). The following theorem (proof omitted) confirms this observation:

For E_u+E_L assumed even, it is the case that:
EQ (19)

Using (15) through (19) it can be verified that the complexity required when using the improved TAFDEC with the optimal misalignment is approximately one-half that required for the prior art (i.e., the zero misalignment case).

Referring to Fig. 7 an ASDL Central Office DMT transceiver (ATU-C) 120, having a low receive rate and a high transmit rate, uses a shared-FFT 122 for TAFDEC processing. Fig. 7 demonstrates how the improved shared-FFT TAFDEC processing can be applied to any asymmetric DMT transceiver which contains a low speed receiver and a high speed transmitter.

The downstream Cyclic Prefix length is similarly the last thirty-two high-speed samples from the downstream IFFT. The analysis of this structure for the ATU-C is very similar to the analysis for the ATU-R 100, described above. (See, for example, D. C. Jones, "Minimizing the Complexity of the ATU-C Echo Canceler," ANSI T1E1.4/93-284, November 15, 1993.) The result is that for a misalignment of Ψ at the ATU-C, the CES for the improved TAFDEC being described here functions by forming the output:

$$\gamma_k^n = \alpha_k^n - \beta_k^n, \; 0 \le k \le 63 \tag{20}$$

where

$$\beta_k^n = \sum_{m=E_L}^{\min(8k+\Psi_n-512,E_U)} h_{echo_m}(\tilde{x}_{8k+\Psi_n-544-m}^{n+1} - \tilde{x}_{8k+\Psi_n-512-m}^{n}) + \sum_{m=\max(8k+\Psi_n+33,E_L)}^{E_U} h_{echo_m}(\tilde{x}_{8k+\Psi_n+544-m}^{n-1} - \tilde{x}_{8k+\Psi_n+512-m}^{n}), \; 0 \le k \le 63 \tag{21}$$

The FDEC functions by forming the output:

$$\Lambda_k^n = \Gamma_k^n - \frac{1}{8}\sum_{m=0}^{7} e^{+j2\pi\Psi_n(k+64m)/512} H_{echo_{k+64m}} X_{k+64m}^n, \; 0 \le k \le 32 \tag{22}$$

LMS updating of the echo path estimate is according to:

$$\hat{H}_{echo_{64m+k}}^{n+1} = \hat{H}_{echo_{64m+k}}^{n} + \mu X_{64m+k}^{n*} \Lambda_k^n e^{-j2\pi\Psi_n(k+64m)/512}, \; 0 \le k \le 63, \; 0 \le m \le 7 \tag{23}$$

The differences between (20)-(23) for the shared-FFT ATU-C 120 and (15)-(18) for the ATU-R 100 are due to the opposite multi-rate situations at the two transceivers. The transceiver 120 uses a CES 124 similar to the CES 112 of FIG. 5.

Referring to FIG. 8, the complexity equations for the CES 124 of the shared-FFT ATU-C 120 are similar to those already derived for the ATU-R 100, as shown in the plot. As was true for the ATU-R 100, the complexity of the ATU-C shared-FFT CES 124 can, in principle, be minimized through optimal misalignment of the phase of S/P_α relative to that of P/S_X. To do this, the designer would select the optimizing misalignment Ψ and implement that offset by causing the equation:

$$(n_R, k_R) = \begin{cases} \left(n_T - 1, \left\lfloor \frac{k_T - \Psi + 544}{8} \right\rfloor \right), & k_T \le \Psi - 33 \\ \left(n_T, \left\lfloor \frac{k_T - \Psi}{8} \right\rfloor \right), & \Psi - 32 \le k_T \le \Psi + 511 \\ \left(n_T + 1, \left\lfloor \frac{k_T - \Psi - 544}{8} \right\rfloor \right), & k_T \ge \Psi + 512 \end{cases} \quad (24)$$

to hold.

However, the transmit/receive symbol misalignment can only be specified by the designer for one of the two transceivers in a link, not both. If the Remote Transceiver is designed to operate at a certain fixed misalignment, then the misalignment at the Central Office Transceiver equals the opposite of the Remote misalignment, plus an amount equal to the channel delay. The opposite is true if the designer selects a fixed transmit/receive symbol misalignment for the Central Office Transceiver. If, for example, the Remote transceiver is designed to use a misalignment of $\Psi = 100$, and the channel connecting the two transceivers has zero delay, then the transmit/receive symbol misalignment at the Central Office Transceiver is $\Psi = -100$,. As indicated by Fig. 8, this results in a much greater TAFDEC complexity for the Central Office Transceiver than for the Remote Transceiver. If instead the Central Office Transceiver were designed with its misalignment fixed at the optimal value, then the Remote Transceiver would experience the required increase in complexity.

Referring to FIG. 9, an ATU-C transceiver 130 uses separate-FFT TAFDEC processing. The separate-FFT TAFDEC provides the designer the ability to optimally misalign the phase of the echo canceler block boundary relative to the transmit symbol boundary. Fig. 9 illustrates how the improved separate-FFT TAFDEC described herein can be applied to any asymmetric DMT transceiver.

In the prior art separate-FFT TAFDEC, the phase of P/S_X, P/S_D, and S/P_E were all assumed to be equal. It is possible to misalign the phase of S/P_E and P/S_D (i.e., the echo canceler block) relative to that of P/S_X (i.e., the transmit symbol). Furthermore, it is possible to make the transceiver properly work in the presence of such echo canceler block/transmit symbol misalignment. It will also be shown that a substantial performance advantage results from using the misaligned structure, compared to the prior art.

In the separate-FFT TAFDEC structure, the misalignment between the echo canceler block and the transmit symbol boundaries can be selected independently of the misalignment between the transmit and receive symbol boundaries. Denote now the misalignment between the transmit symbol and echo canceler block boundaries as Ψ, measured in high speed samples. The misalignment between the transmit and receive symbol boundaries is, in general, some other number, and is not important to the operation of the TAFDEC described now. The echo canceler block/transmit symbol misalignment of Ψ is implemented by the designer by implementing the following relation between the echo canceler and transmitter subscript/superscript pairs:

$$(n_E, k_E) = \begin{cases} \left(n_T - 1, \left\lfloor \frac{k_T - \Psi + 544}{8} \right\rfloor\right), & k_T \le \Psi - 33 \\ \left(n_T, \left\lfloor \frac{k_T - \Psi}{8} \right\rfloor\right) & \Psi - 32 \le k_T \le \Psi + 511 \\ \left(n_T + 1, \left\lfloor \frac{k_T - \Psi - 511}{8} \right\rfloor\right), & k_T \ge \Psi + 512 \end{cases} \quad (25)$$

This misalignment manifests itself in Figure 9 as follows: If $\Psi \ge -32$ samples, then the relative phase between P/S_D and P/S_X is such that the output of P/S_X is $\bar{x}_{\Psi}^{n}$ at the same time that d_0^{-n} is newly output from P/S_D. If $\Psi \le -33$, then $X_{544+\Psi}^{-n-1}$ is the P/S_X output when d_0^{-n} is newly at the output of P/S_D. With an echo canceler/transmit symbol misalignment of Ψ in place, the improved separate-FFT TAFDEC of Fig. 9 operates as follows: The CES forms the quantity:

$$\mu_{k_E}^{n_E} = c_{68n_E+k_E} - p_{k_E}^{n_E}, \quad -4 \le k_E \le 63 \quad (26)$$

where

$$p_{k_E}^{n_E} = \sum_{m=E_L}^{\min(8k_E+\Psi-512, E_U)} h_{echo_m} (\bar{x}_{8k_E+\Psi-544-m}^{n_E+1} - \bar{x}_{8k_E+\Psi-512-m}^{n_E}) + \sum_{m=\max(8k_E-\Psi+33, E_L)}^{E_U} h_{echo_m} (\bar{x}_{8k_E+\Psi+544-m}^{n_E-1} - \bar{x}_{8k_E+\Psi+512-m}^{n_E}), \quad -4 \le k_E \le 63 \quad (27)$$

The frequency domain portion of the TAFDEC computes:

$$D_{k_E}^{n_E} = \frac{1}{8} \sum_{m=0}^{7} e^{+j2\pi\Psi(k_E+64m)/512} H_{echo_{k_E+64m}} X_{k_E+64m}^{n_E}, \quad 0 \le k_E \le 63 \quad (28)$$

and then forms the points $d_{k_E}^{n_E}$ as shown. $E_{k_E}^{n_E}$ is also formed as indicated , and used to update the estimate of the echo impulse response required by the TAFDEC according to:

$$\hat{H}^{n+1}_{echo_{64m+k}} = \hat{H}^{n}_{echo_{64m+k}} + \mu X^{n*}_{64m+k} E^{n}_{k} e^{-j2\pi\Psi(k+64m)/512},\ 0 \le k \le 63,\ 0 \le m \le 7 \qquad (29)$$

Referring to FIG. 10, a plot shows the complexity of the ATU-C separate-FFT CES 130 as a function of canceler/transmitter misalignment. As can be seen from Fig. 10, the ability of the improved TAFDEC to work with any canceler/transmitter misalignment approximately doubles the achievable performance, relative to that of the prior art (i.e., zero misalignment).

Thus far the concepts in this report have been described in terms of Asymmetric Digital Subscriber Lines (ADSL). However, this invention can be used with similar performance improvement in any symmetric transmission system as well.

Fig. 11 shows a symmetric transceiver 140 which utilizes an improved shared-FFT TAFDEC. This invention can be applied to any full-duplex symmetric DMT transceiver.

The TAFDEC symmetric transceiver 140 operates as follows: The designer establishes a misalignment of Ψ samples between the transmit and receive symbol boundaries by setting the relative phase between P/S_U and S/P_G such that:

$$(n_T, k_T) = \begin{cases} (n_R - 1, k_R + \Psi + N - \upsilon), & k_R \le -\upsilon - \Psi - 1 \\ (n_R, k_R + \Psi), & -\upsilon - \Psi \le k_R \le N - 1 - \Psi \\ (n_R + 1, k_R + \Psi - N - \upsilon), & k_R \ge N - \Psi \end{cases} \qquad (30)$$

A CES 142 of the transceiver operates by forming at the output:

$$q^{n}_{k} = g^{n}_{k} - \varepsilon^{n}_{k},\ 0 \le k \le N-1 \qquad (31)$$

where by definition:

$$\varepsilon_k^n = \sum_{m=E_L}^{\min(E_U,\,k+\Psi_n-N)} h_{echo_m}(\tilde{u}_{k+\Psi_n-m-N-\upsilon}^{n+1} - \tilde{u}_{k+\Psi_n-m-N}^{n}$$

$$+ \sum_{m=\max(E_L,\,k+\Psi_n+\upsilon+1)}^{E_U} h_{echo_m}(\tilde{u}_{k+\Psi_n-m+N+\upsilon}^{n-1} - \tilde{u}_{k+\Psi_n-m+N}^{n},\ 0 \le k \le N-1 \qquad (32)$$

An FDEC 144 of the transceiver 140 operates by forming the output:

$$W_k^n = Q_k^n - e^{+j2\pi k\Psi_n/N} H_{echo_k} U_k^n,\ 0 \le k \le N/2 \qquad (33)$$

The echo impulse response estimate is updated according to:

$$\hat{H}_{echo_m}^{n+1} = \hat{H}_{echo_m}^{n} + \mu e^{-j2\pi\Psi_n m/N} U_m^{n*} W_m^n,\ 0 \le m \le N-1 \qquad (34)$$

In a manner similar to that demonstrated with respect to Fig. 6, the performance of the new TAFDEC for the transceiver 140 is approximately twice that available from the prior art, the prior art being a symmetric shared-FFT TAFDEC with zero misalignment.

Referring to FIG. 12, a symmetric transceiver 150, which utilizes an improved separate-FFT TAFDEC, can be applied to any full-duplex symmetric DMT transceiver. The TAFDEC processing of the transceiver 150 operates as follows: The designer establishes a misalignment of Ψ samples between the

transmit symbol and echo canceler block boundaries by setting the relative phase between P/S_X and P/S_D such that:

$$(n_E,k_E) = \begin{cases} (n_T-1,k_T-\Psi+N+\upsilon), & k_T\le\Psi-\upsilon-1 \\ (n_T,k_T-\Psi), & \Psi-\upsilon\le k_T\le\Psi+N-1 \\ (n_T+1,k_T-\Psi-N-\upsilon), & k_T\ge\Psi+N \end{cases} \quad (35)$$

A CES 152 of the transceiver 150 operates by forming the output:

$$\mu_{k_E}^{n_E} = c_{(N+\upsilon)n_E+k_E} - \rho_{k_E}^{n_E},\ -\upsilon\le k_E\le N-1 \quad (36)$$

where by definition:

$$\rho_k^n = \sum_{m=E_L}^{\min(E_U,k+\Psi-N)} h_{echo_m}(\bar{x}_{k+\Psi-m-N-\upsilon}^{n+1} - \bar{x}_{k+\Psi-m-N}^{n})$$

$$+ \sum_{m=\max(E_L,k+\Psi+\upsilon+1)}^{E_U} h_{echo_m}(\bar{x}_{k+\Psi-m+N+\upsilon}^{n-1} - \bar{x}_{k+\Psi-m+N}^{n}),\ -\upsilon\le k\le N-1 \quad (37)$$

The frequency domain portion of the TAFDEC processing of the transceiver 150 operates as shown in Fig. 12, where D_k^n is computed by the canceler according to:

$$D_k^n = X_k^n H_{echo_k} e^{+j2\pi k\Psi/N},\ 0\le k\le N-1 \quad (38)$$

The estimate of the echo impulse response used by the TAFDEC processing of the transceiver 150 is updated according to:

$$\hat{H}_{echo_m}^{n+1} = \hat{H}_{echo_m}^{n} + \mu X_m^{n^*} E_m^n e^{-j2\pi\Psi m/N}, \quad 0 \le m \le N-1 \tag{39}$$

Modifications and variations of the above-described embodiments of the present invention are possible, as appreciated by those skilled in the art in light of the above teachings. It is therefore to be understood that, within the scope of the appended claims and their equivalents, the invention may be practiced otherwise than as specifically described.

What is claimed is:

1. An asymmetric Digital Multitone transceiver, for transmitting for receiving digital messages on the same channel, comprising:

a hybrid, coupled to the channel;

a transmitter, including a parallel to serial converter and a D/A converter that samples at a first rate, said transmitter coupled to the hybrid to provide message signals to the hybrid;

an echo canceler, coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a received message signal, said echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, said echo canceler subtracting, in the frequency domain, a signal indicative of a signal provided by said transmitter; and

a receiver, including a serial to parallel converter and an A/D converter that samples at a second rate lower than said first rate, said receiver coupled to the echo canceler to provide an output signal,

wherein said serial to parallel and parallel to serial converters are set to provide a non-zero phase difference between signals of said transmitter and receiver and wherein the phase shift and multiply provided by said echo canceler compensate for said phase difference.

2. An asymmetric Digital Multitone transceiver, according to claim 1, wherein the phase difference is set to a value that minimizes the complexity of the echo canceler.

3. An asymmetric Digital Multitone transceiver, for transmitting and receiving digital messages on the same channel, comprising:

a hybrid, coupled to the channel;

a transmitter, including a parallel to serial converter and a D/A converter that samples at a first rate, said transmitter coupled to the hybrid to provide message signals to the hybrid;

an echo canceler, coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a received message signal, said echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, said echo canceler subtracting, in the frequency domain, a signal indicative of a signal provided by said transmitter; and

a receiver, including a serial to parallel converter and an A/D converter that samples at a second rate higher than said first rate, said receiver coupled to the echo canceler to provide an output signal,

wherein said serial to parallel and parallel to serial converters are set to provide a non-zero phase difference between signals of said transmitter and receiver and wherein the phase shift and multiply provided by said echo canceler compensate for said phase difference.

4. An asymmetric Digital Multitone transceiver, according to claim 3, wherein the phase difference is set to a value that minimizes the complexity of the echo canceler.

5. A symmetric Digital Multitone transceiver, for transmitting and receiving digital messages on the same channel, comprising:

a hybrid, coupled to the channel;

a transmitter, including a parallel to serial converter and a D/A converter that samples at a first rate, said transmitter coupled to the hybrid to provide message signals to the hybrid;

an echo canceler, coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a

received message signal, said echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, said echo canceler subtracting, in the frequency domain, a signal indicative of a signal provided by said transmitter; and

a receiver, including a serial to parallel converter and an A/D converter that samples at a second rate equal to said first rate, said receiver coupled to the echo canceler to provide an output signal,

wherein said serial to parallel and parallel to serial converters are set to provide a non-zero phase difference between signals of said transmitter and receiver and wherein the phase shift and multiply provided by said echo canceler compensate for said phase difference.

6. A symmetric Digital Multitone transceiver, according to claim 5, wherein the phase difference is set to a value that minimizes the complexity of the echo canceler.

7. An asymmetric Digital Multitone transceiver, for transmitting and receiving digital messages on the same channel, comprising:

a hybrid, coupled to the channel;

a transmitter, including a parallel to serial converter and a D/A converter that samples at a first rate, said transmitter coupled to the hybrid to provide message signals to the hybrid;

an echo canceler, including a serial to parallel converter, said echo canceler coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a received message signal, said echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, said echo canceler subtracting, in the time domain, a signal indicative of a signal provided by said transmitter; and

a receiver, including an A/D converter that samples at a second rate higher than said first rate, said receiver coupled to the echo canceler to provide an output signal,

wherein said serial to parallel and parallel to serial converters are set to provide a non-zero phase difference between signals of said transmitter and said echo canceler and wherein the phase shift and multiply provided by said echo canceler compensate for said phase difference.

8. An asymmetric Digital Multitone transceiver, according to claim 7, wherein the phase difference is set to a value that minimizes the complexity of the echo canceler.

9. An asymmetric Digital Multitone transceiver, for transmitting and receiving digital messages on the same channel sampled, comprising:

a hybrid, coupled to the channel;

a transmitter, including a parallel to serial converter and a D/A converter that samples at a first rate, coupled to the hybrid to provide message signals to the hybrid;

an echo canceler, including a serial to parallel converter, said echo canceler coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a received message signal, said echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, said echo canceler subtracting, in the time domain, a signal indicative of a signal provided by said transmitter; and

a receiver, including an A/D converter that samples at a second rate lower than said first rate, said receiver coupled to the echo canceler to provide an output signal,

wherein said serial to parallel and parallel to serial converters are set to provide a non-zero phase difference between signals of said transmitter and said echo canceler and

wherein the phase shift and multiply provided by said echo canceler compensate for said phase difference.

10. An asymmetric Digital Multitone transceiver, according to claim 9, wherein the phase difference is set to a value that minimizes the complexity of the echo canceler.

11. A symmetric Digital Multitone transceiver, for transmitting and receiving digital messages on the same channel comprising:

a hybrid, coupled to the channel;

a transmitter, including a parallel to serial converter and a D/A converter that samples at a first rate, said transmitter coupled to the hybrid to provide message signals to the hybrid;

an echo canceler, including a serial to parallel converter, said echo canceler coupled to the transmitter to access a transmit message signal and coupled to the hybrid to accept a received message signal, said echo canceler performing a phase shift in the time domain and a multiply in the frequency domain on the transmit message signal, said echo canceler subtracting, in the time domain, a signal indicative of a signal provided by said transmitter; and

a receiver, including an A/D converter that samples at a second rate equal to said first rate, said receiver coupled to the echo canceler to provide an output signal,

wherein said serial to parallel and parallel to serial converters are set to provide a non-zero phase difference between signals of said transmitter and said echo canceler and wherein the phase shift and multiply provided by said echo canceler compensate for said phase difference.

12. An asymmetric Digital Multitone transceiver, according to claim 11, wherein the phase difference is set to a value that minimizes the complexity of the echo canceler.

13. A method of canceling echo in a Digital Multitone transceiver, the transceiver including a hybrid, a transmitter with a parallel to serial converter and an D/A converter, an echo canceler coupled to the transmitter and the hybrid, and a receiver having a serial to parallel converter and an A/D converter, the method comprising the steps of:

performing a phase shift in the time domain and a multiply in the frequency domain on a transmit message signal;

subtracting, in the frequency domain, a signal indicative of a signal provided by the transmitter; and

setting the serial to parallel and parallel to serial converters to provide a non-zero phase difference between signals of the transmitter and receiver wherein the phase shift and multiply steps compensate for said phase difference.

14. A method of canceling echo in a Digital Multitone transceiver, according to claim 13, further including the step of:

setting the phase difference to a value that minimizes the complexity of the echo canceler.

15. A method of canceling echo in a Digital Multitone transceiver, according to claim 13, further including the step of:

setting the sample rate of the D/A converter higher than the sample rate of the A/D converter.

16. A method of canceling echo in a Digital Multitone transceiver, according to claim 13, further including the step of:

setting the sample rate of the D/A converter lower than the sample rate of the A/D converter.

17. A method of canceling echo in a Digital Multitone transceiver, according to claim 13, further including the step of:

setting the sample rate of the D/A converter equal to the sample rate of the A/D converter.

18. A method of canceling echo in a Digital Multitone transceiver, according to claim 14, further including the step of:

setting the sample rate of the D/A converter higher than the sample rate of the A/D converter.

19. A method of canceling echo in a Digital Multitone transceiver, according to claim 14, further including the step of:

setting the sample rate of the D/A converter lower than the sample rate of the A/D converter.

20. A method of canceling echo in a Digital Multitone transceiver, according to claim 14, further including the step of:

setting the sample rate of the D/A converter equal to the sample rate of the A/D converter.

21. A method of canceling echo in a Digital Multitone transceiver, the transceiver including a hybrid, a transmitter with a parallel to serial converter and an D/A converter, an echo canceler having a serial to parallel converter and being coupled to the transmitter and the hybrid, and a receiver having an A/D converter, the method comprising the steps of:

performing a phase shift in the time domain and a multiply in the frequency domain on a transmit message signal;

subtracting, in the time domain, a signal indicative of a signal provided by the transmitter; and

setting the serial to parallel and parallel to serial converters to provide a non-zero phase difference between signals of the transmitter and the echo canceler wherein the phase shift and multiply steps compensate for said phase difference.

22. A method of canceling echo in a Digital Multitone transceiver, according to claim 21, further including the step of:

setting the phase difference to a value that minimizes the complexity of the echo canceler.

23. A method of canceling echo in a Digital Multitone transceiver, according to claim 21, further including the step of:

setting the sample rate of the D/A converter higher than the sample rate of the A/D converter.

24. A method of canceling echo in a Digital Multitone transceiver, according to claim 21, further including the step of:

setting the sample rate of the D/A converter lower than the sample rate of the A/D converter.

25. A method of canceling echo in a Digital Multitone transceiver, according to claim 21, further including the step of:

setting the sample rate of the D/A converter equal to the sample rate of the A/D converter.

26. A method of canceling echo in a Digital Multitone transceiver, according to claim 22, further including the step of:

setting the sample rate of the D/A converter higher than the sample rate of the A/D converter.

27. A method of canceling echo in a Digital Multitone transceiver, according to claim 22, further including the step of:

setting the sample rate of the D/A converter lower than the sample rate of the A/D converter.

28. A method of canceling echo in a Digital Multitone transceiver, according to claim 22, further including the step of:

setting the sample rate of the D/A converter equal to the sample rate of the A/D converter.

FIG. 1

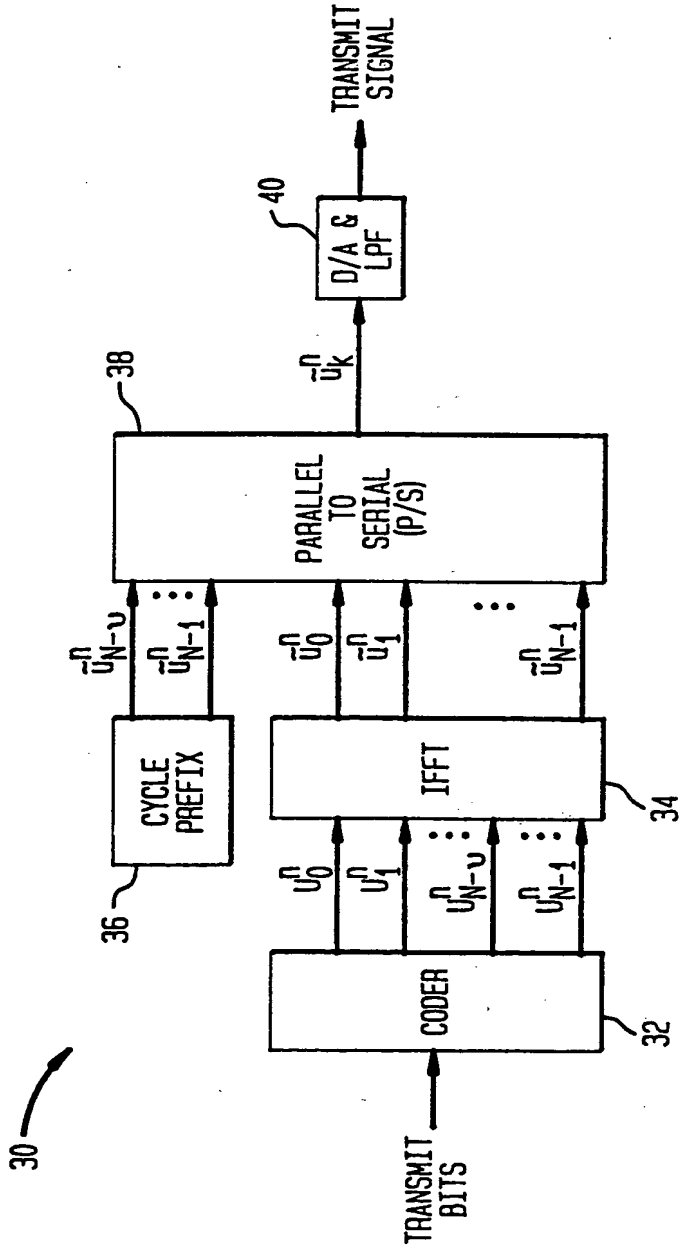

TRANSMIT SIGNAL
40
D/A & LPF
38
PARALLEL TO SERIAL (P/S)
CYCLE PREFIX
36
IFFT
34
CODER
32
TRANSMIT BITS
30

FIG. 2

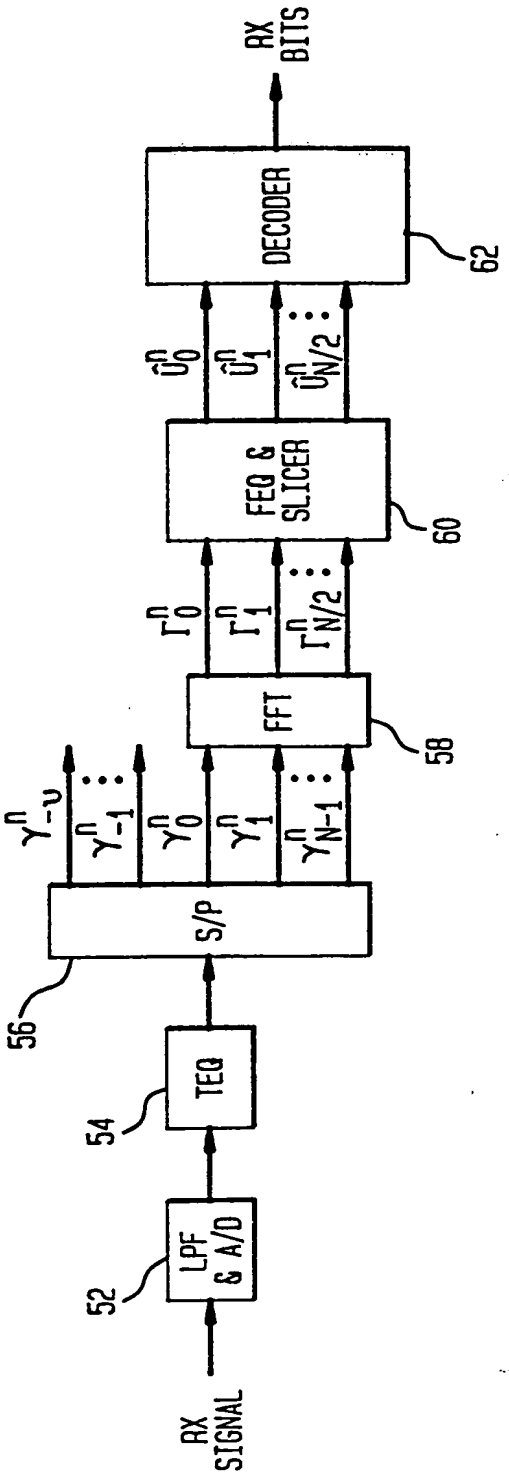

RX SIGNAL
LPF & A/D
52
TEQ
54
S/P
56
FFT
58
FEQ & SLICER
60
DECODER
62
RX BITS

FIG. 3

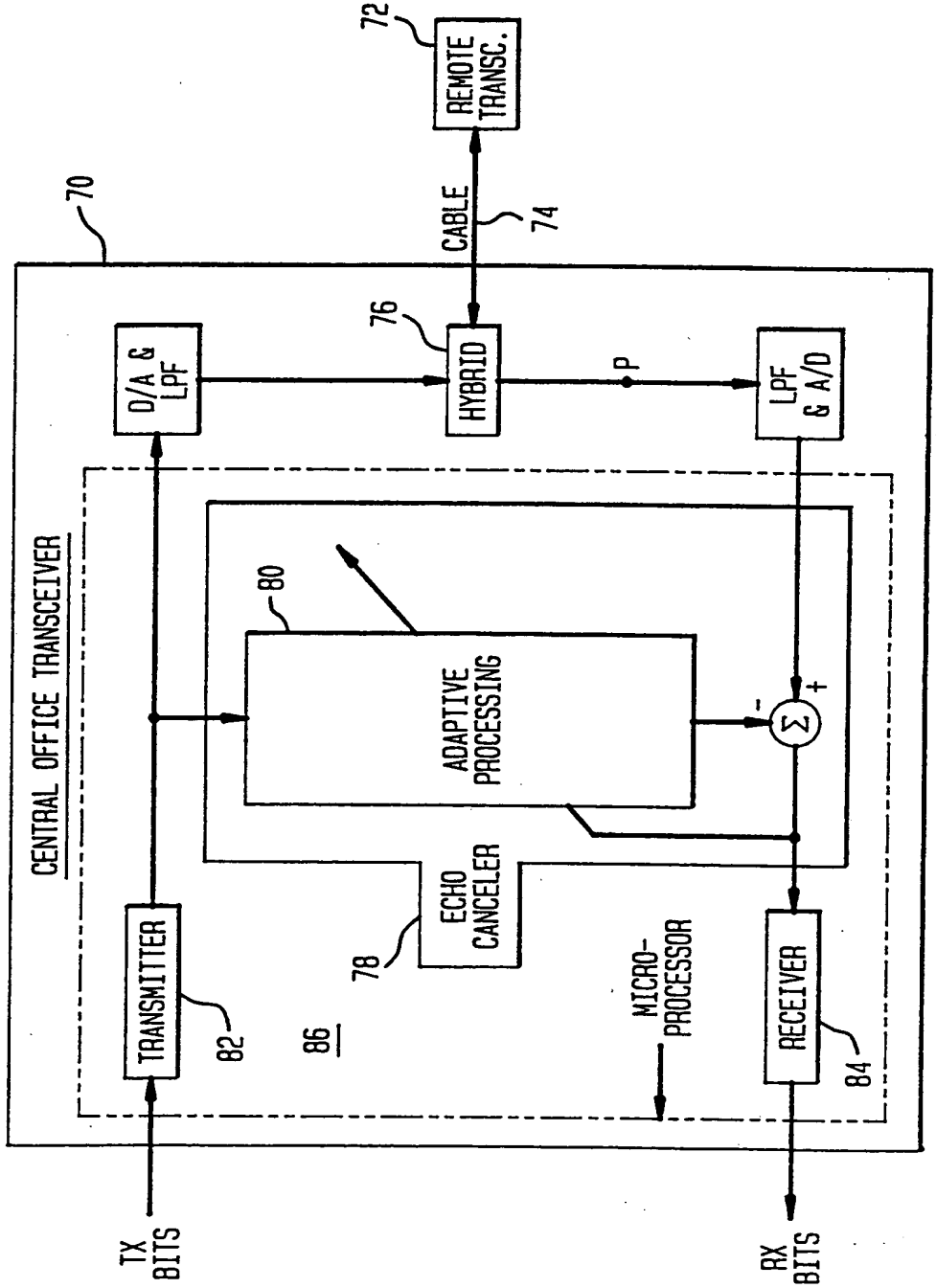

72
REMOTE TRANSC.
CABLE
74
70
76
HYBRID
D/A & LPF
P
LPF & A/D
CENTRAL OFFICE TRANSCEIVER
80
ADAPTIVE PROCESSING
Σ
-
+
ECHO CANCELER
78
TRANSMITTER
82
86
MICRO-PROCESSOR
RECEIVER
84
TX BITS
RX BITS

FIG. 4

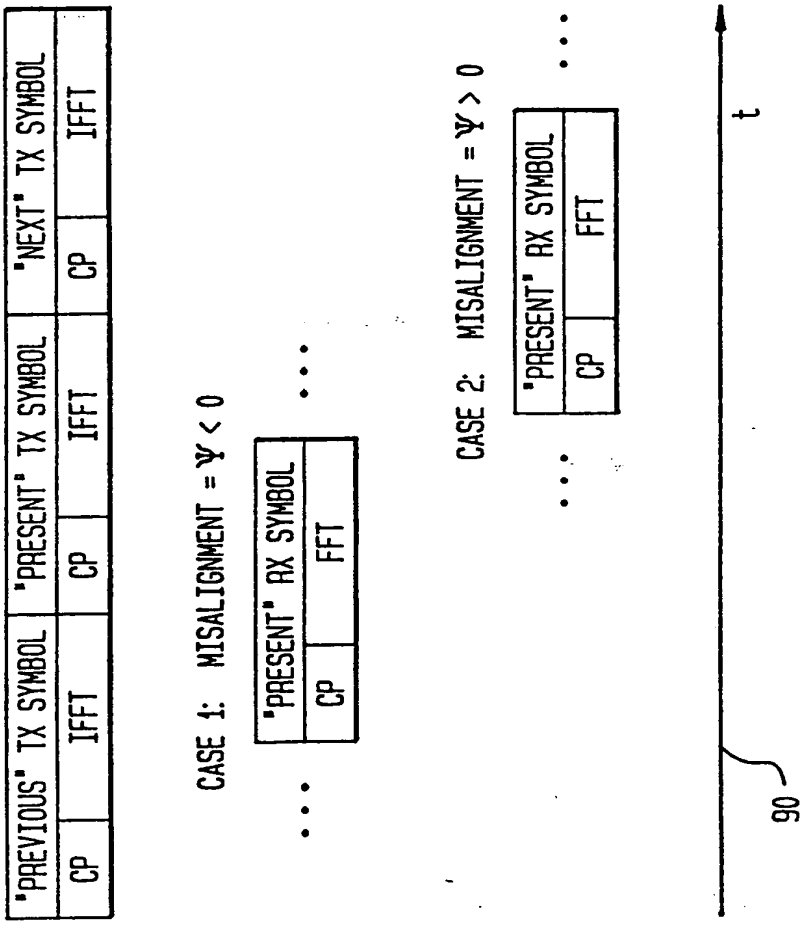

'PREVIOUS' TX SYMBOL
CP
IFFT
'PRESENT' TX SYMBOL
CP
IFFT
'NEXT' TX SYMBOL
CP
IFFT
CASE 1: MISALIGNMENT = Ψ < 0
'PRESENT' RX SYMBOL
CP
FFT
CASE 2: MISALIGNMENT = Ψ > 0
'PRESENT' RX SYMBOL
CP
FFT
t
90

FIG. 5

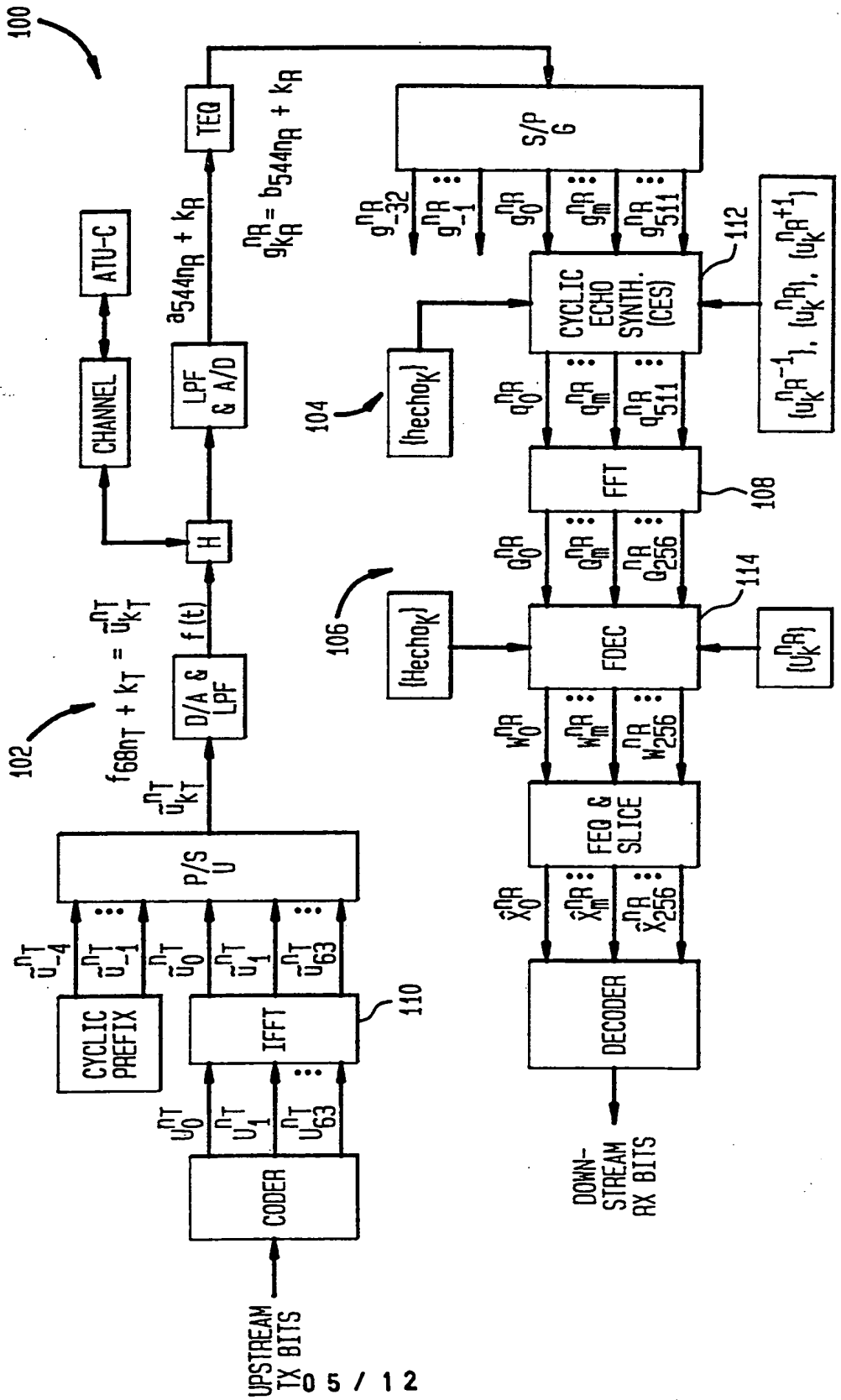

100
102
104
106
108
110
112
114
UPSTREAM TX BITS
CODER
IFFT
CYCLIC PREFIX
P/S U
D/A & LPF
H
CHANNEL
ATU-C
LPF & A/D
TEQ
S/P G
CYCLIC ECHO SYNTH. (CES)
FFT
FDEC
FEQ & SLICE
DECODER
DOWN-STREAM RX BITS

FIG. 6

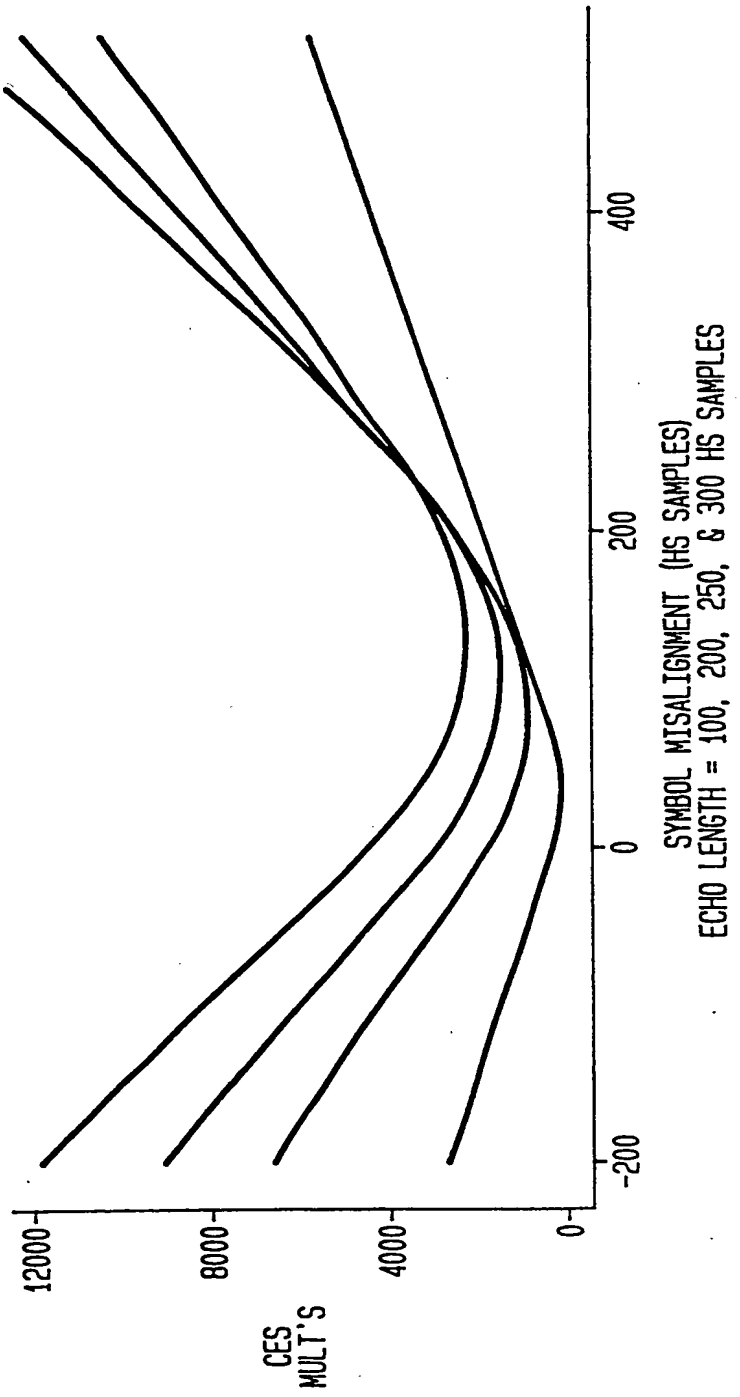

12000
8000
4000
0
CES MULT'S
-200
0
200
400
SYMBOL MISALIGNMENT (HS SAMPLES)
ECHO LENGTH = 100, 200, 250, & 300 HS SAMPLES

FIG. 7

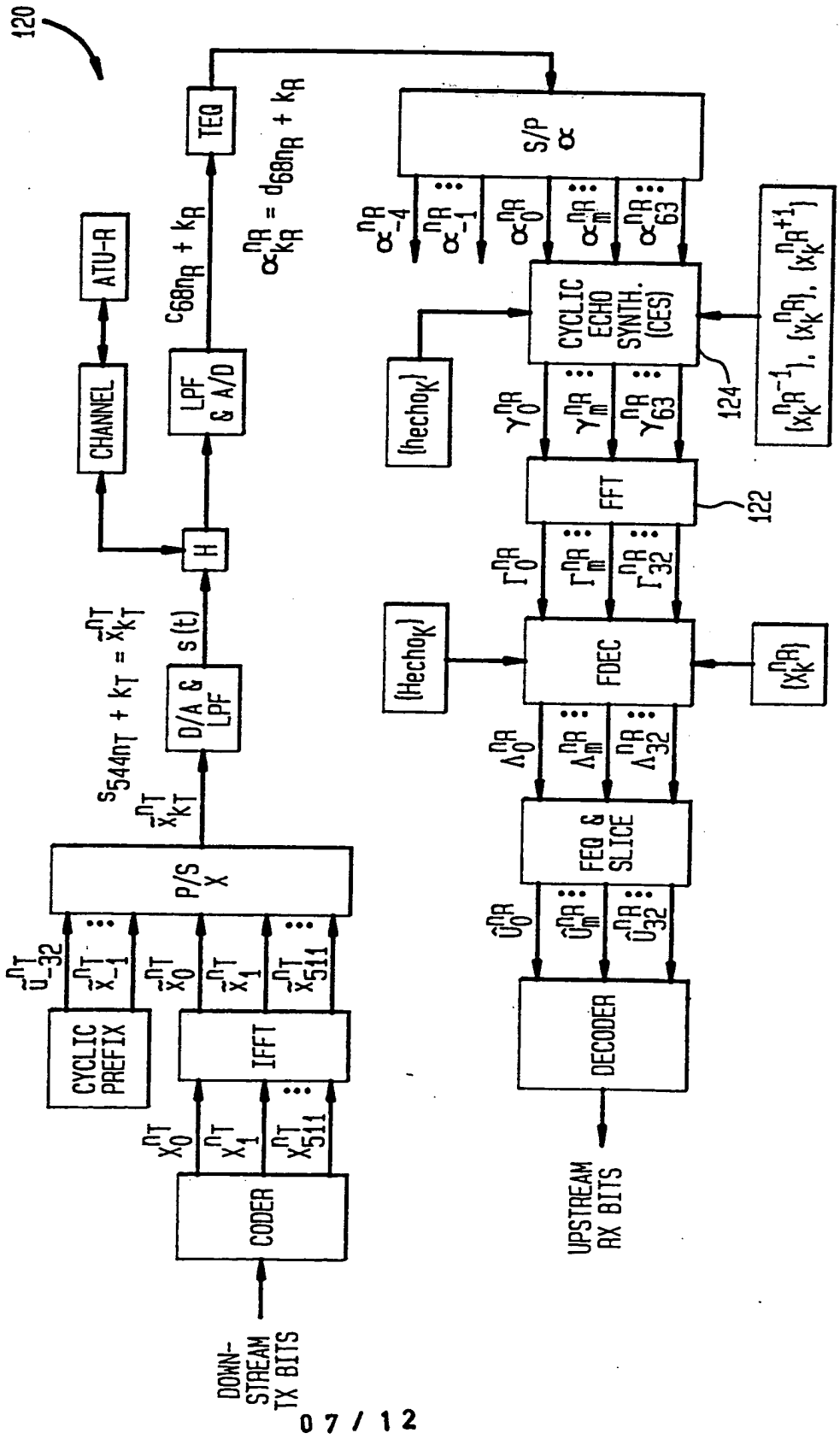

120
DOWN-STREAM TX BITS
CODER
IFFT
CYCLIC PREFIX
P/S
D/A & LPF
H
CHANNEL
ATU-R
LPF & A/D
TEQ
S/P
CYCLIC ECHO SYNTH. (CES)
124
FFT
122
FDEQ
FEQ & SLICE
DECODER
UPSTREAM RX BITS

FIG. 8

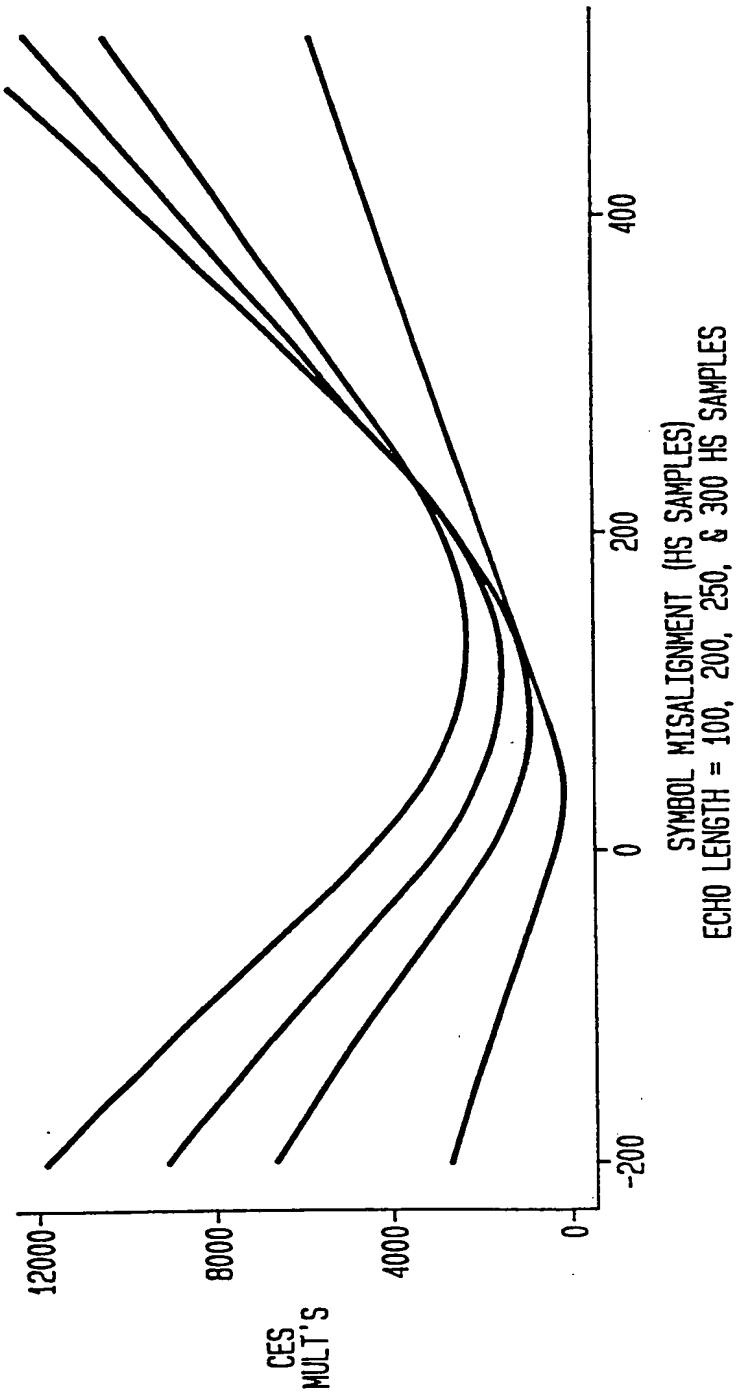

12000
8000
4000
0
CES MULT'S
-200
0
200
400
SYMBOL MISALIGNMENT (HS SAMPLES)
ECHO LENGTH = 100, 200, 250, & 300 HS SAMPLES

FIG. 9

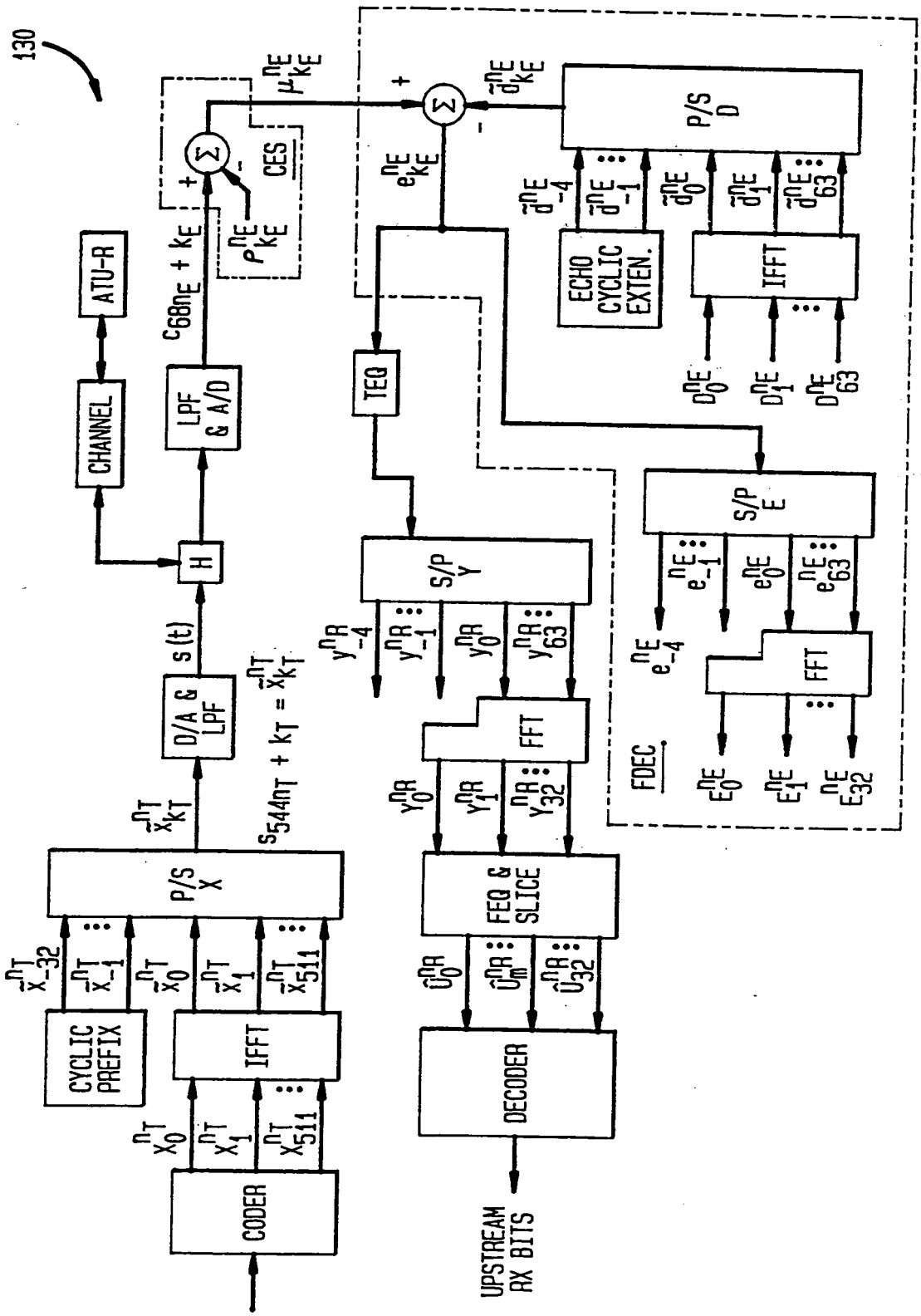

130
DOWN-STREAM TX BITS
CODER
IFFT
CYCLIC PREFIX
P/S X
D/A & LPF
s(t)
H
CHANNEL
ATU-R
LPF & A/D
CES
TEQ
S/P Y
FFT
FEQ & SLICE
DECODER
UPSTREAM RX BITS
FDEC
S/P E
FFT
P/S D
IFFT
ECHO CYCLIC EXTEN.

FIG. 10

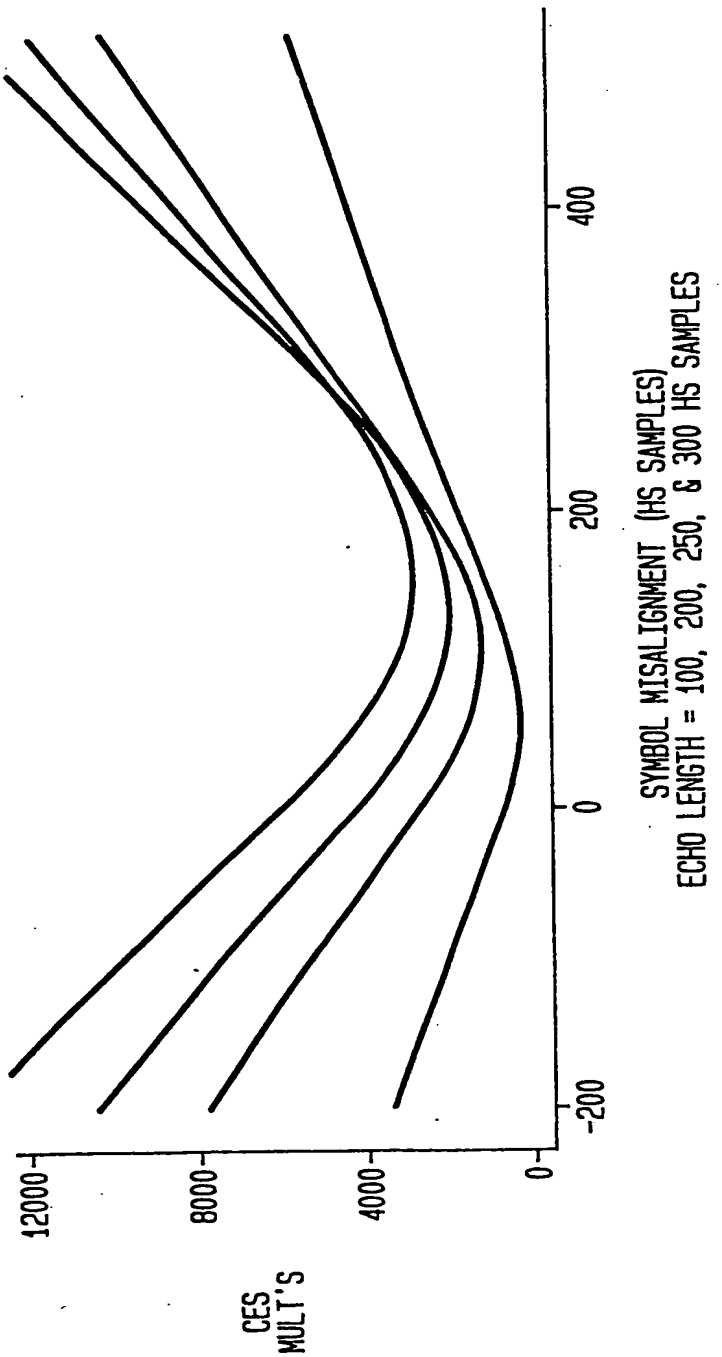
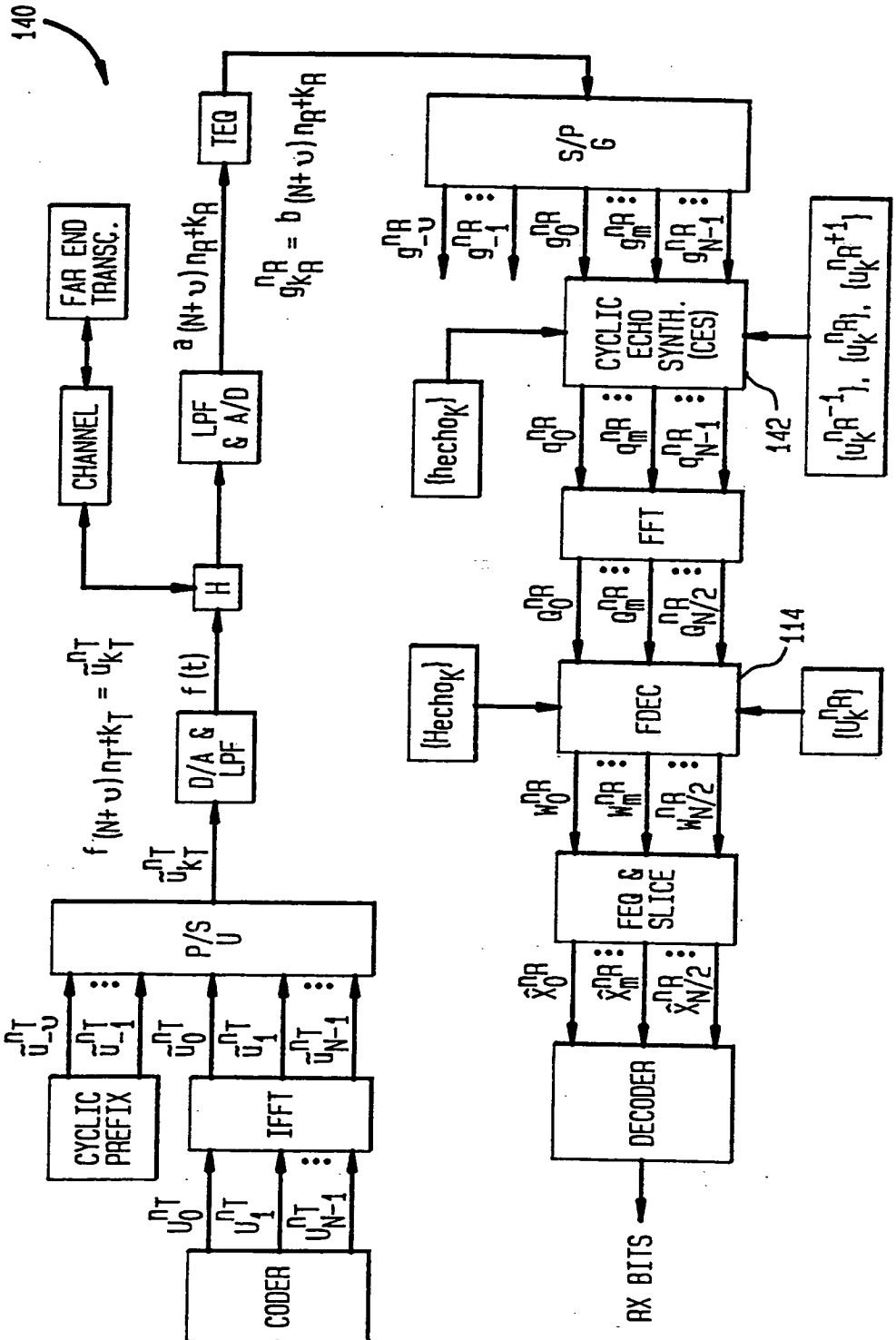

12000
8000
4000
0
CES MULT'S
-200
0
200
400
SYMBOL MISALIGNMENT (HS SAMPLES)
ECHO LENGTH = 100, 200, 250, & 300 HS SAMPLES

FIG. 11


140
TX BITS
CODER
IFFT
CYCLIC PREFIX
P/S U
D/A & LPF
H
CHANNEL
FAR END TRANSC.
LPF & A/D
TEQ
S/P G
CYCLIC ECHO SYNTH. (CES)
142
FFT
FDEC
114
FEQ & SLICE
DECODER
RX BITS

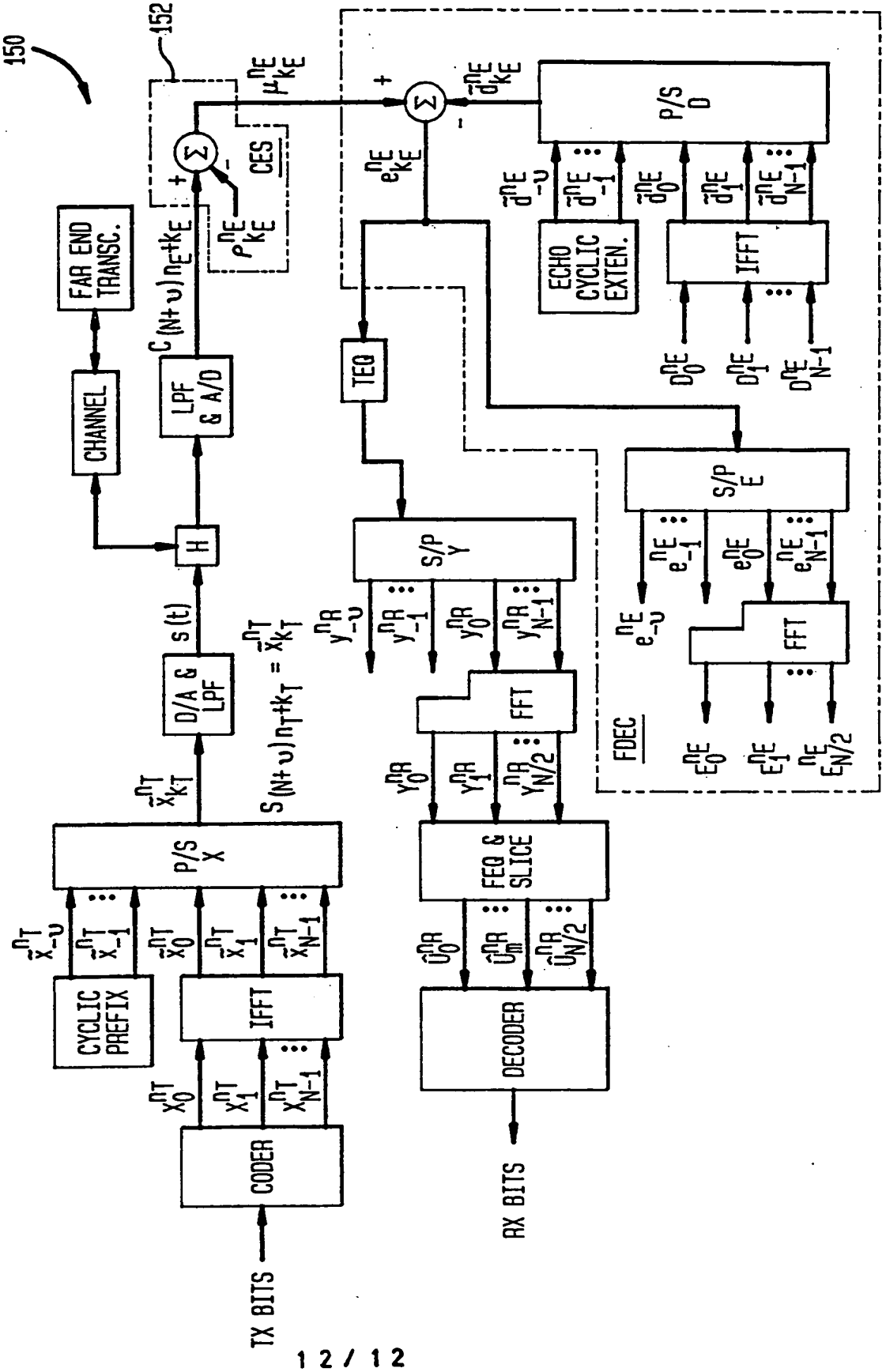

150
152
TX BITS
CODER
IFFT
CYCLIC PREFIX
P/S X
D/A & LPF
s(t)
H
CHANNEL
FAR END TRANSC.
LPF & A/D
CES
ECHO CANCELLER
TEQ
S/P Y
FFT
FEQ & SLICE
DECODER
RX BITS
P/S D
IFFT
ECHO CYCLIC EXTEN.
S/P E
FFT
FDEC

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/14250

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04B 1/38; H03H 7/30; H04M 1/24; H04J 1/00
US CL : 375/07, 103; 379/3; 370/32.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/07, 14, 58, 103; 379/3, 410, 411; 370/17, 24, 32, 32.1; 455/69, 127

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS: digital multitone, echo canceler, asymmetric, symmetric, transceiver, hybrid.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, P	US, A, 5,317,596 (HO et al) 31 May 1994, col 5, line 26 to col 9, line 59.	1-28

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
06 MARCH 1995	15MAY1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MADELEINE NGUYEN Telephone No. (703) 305-4860

Form PCT/ISA/210 (second sheet)(July 1992)*